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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/606,252	06/28/2000	Raminda U. Madurawe	A293D	5633

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EXAMINER

BROCK II, PAUL E

ART UNIT	PAPER NUMBER
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2815

DATE MAILED: 03/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/606,252	Applicant(s) MADURAWA ET AL.	
	Examiner Paul E Brock II	Art Unit 2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 03 February 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 27, 29-38, 40 and 42-47 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 27, 29-38, 40 and 42-47 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 03 February 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Drawings

1. The proposed drawing correction and/or the proposed substitute sheets of drawings, filed on February 3, 2004 have been approved.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 27, 29 – 31, 33, 34, and 45 – 47 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

It is not clear how a single mask can be used to accomplish depositing a field implant, depositing a well implant and depositing an enhancement implant. Figure 4 and the specification on page 7, lines 7–18 states “Mask region 410 is the mask area defined for formation of well 140, ” and continues to state that “Well 140, field implant 120, and enhancement region 130 (for enhancement transistors) can be formed by implanting at different energy levels, using only the mask defining mask region 410.” The first statement can only lead to the interpretation that

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there is a mask in the area defined by mask region 410 when forming the well 140. How can the well be formed when there is a mask over the area where the well is to be formed? Since there is a mask in the mask region over the to be implanted well region, one of ordinary skill in the art would not recognize that the well region could be implanted. The second statement can be interpreted that this mask is present for the formation of the well 140, field implant 120, and enhancement region 130. Field implant 120 is shown to exist outside the area of the mask, while the well 140, and enhancement region 130 are shown below the mask. One of ordinary skill in the art would not know how a mask can succeed in both blocking implant x (field implant) from area "A" (under the mask) while blocking implants y and z (well and enhancement implants) from area "B" (outside the mask). It does not appear that a single mask could accomplish this function while only "implanting at different energy levels." For these reasons, the specification does not enable one of ordinary skill in the art to accomplish the claim limitation "wherein the implanting the field implant, the well implant, and the enhancement implant are done using a single mask." Further, any suggestion that the originally filed specification discloses using a mask for only the field implant to form region 120 is not persuasive. The disclosed profile of the well region would not suggest to one of ordinary skill in the art that the field oxide regions 150 are used as a mask for the well implant. This is due to the continuous profile of the well region directly under the field oxide regions 150. If the field oxide regions were used as the mask for the well implant there would be a noticeable profile defined by the implant passing through the field oxide region, and there would be no definite boundary of the well region as shown in figures 1a and 4.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 27, 29, 30, 31, 33, and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okumura et al. (USPAT 5763921, Okumura) in view Yuki et al. (USPAT 5466957, Yuki) and Sanchez (USPAT 5583067).

With regard to claim 27, Okumura discloses in figures 2 – 7 a method of fabricating a transistor in an integrated circuit device. Okumura discloses in figure 2 providing a semiconductor substrate (1). Okumura discloses in figure 6 implanting a field implant (63). Okumura discloses in figure 5 implanting a well implant (62). Okumura discloses in figure 4 implanting an enhancement implant (61). Okumura discloses in figure 7 forming a gate oxide (7) on the semiconductor substrate. Okumura discloses in figure 7 forming a gate (8) on the gate oxide. Okumura discloses in figures 4 – 6 wherein the implanting the field implant, the well implant, and the enhancement implant are done using a single mask (4). Okumura does not teach pocket implants. Yuki teaches in figure 3b implanting (22) a first pocket implant (right side 21a) into the semiconductor substrate from a first side of the gate. Yuki teaches in figure 3b implanting a second pocket implant (left side 21a) into the semiconductor substrate from a second side of the gate. Yuki further teaches in figure 3b – 3d wherein the first pocket implant and the second pocket implant are in contact at about the center of a channel region. It would

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have been obvious to one of ordinary skill in the art at the time of the present invention to use the pocket implants of Yuki in the method of Okumura in order to suppress short channel effect while reducing the electric field concentration as stated by Yuki in column 1, lines 47 – 51 and column 4, lines 31 – 41. The pocket implants of Yuki result in an excellent semiconductor device, as Yuki states in column 4, lines 31 – 41. Yuki teaches in column 5, lines 54 – 60 that the pocket implants are boron implants. Okumura and Yuki are silent to the fact that the first pocket implant and the second pocket implant laterally diffuse in the semiconductor substrate. Sanchez teaches in column 7, lines 40 – 45 lateral diffusion of boron. It would have been obvious to one of ordinary skill in the art at the time of the present invention for the pocket implants of Okumura and Yuki to diffuse laterally such as the implants of Sanchez because later process steps will facilitate the diffusion as stated by Sanchez in column 7, lines 40 – 45. It is obvious in the method of Okumura, Yuki, and Sanchez that the lateral diffusion of the pocket implants would adjust a short channel effect of the transistor. Further, it should be noted that the claim limitation “adjusting a short channel effect of the transistor” is an intended use recitation that is not given patentable weight in a method claim.

With regard to claim 29, Yuki teaches in figure 3b the first pocket implant and the second pocket implant are implanted at an angle.

With regard to claim 30, Yuki teaches in figure 3b the first pocket implant and the second pocket-implant are implanted using the gate as a mask.

With regard to claim 31, it should be noted that “wherein the diffusing increases a reverse short channel effect of the transistor” is an intended use limitation that does not bear any

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patentable weight within the method claim. Therefore, Okumura, Yuki, and Sanchez read on the claimed invention.

With regard to claim 33, Yuki teaches in figure 3a – 3d; column 5, lines 51 – 67; and column 6, lines 1 – 11 forming a source on the first side of the gate and a drain on the second side of the gate, wherein the source and drain are doped at a first polarity and the first pocket implant and the second pocket implant are doped at a second polarity.

With regard to claim 34, Yuki teaches in figure 3b – 3d; column 5, lines 51 – 67; and column 6, lines 1 – 11 that the first polarity is different than the second polarity.

6. Claims 35, 36, 38, 40, 42, and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yuki in view of Sanchez.

With regard to claim 35, Yuki discloses in figures 3a – 3d a method of fabricating a transistor in an integrated circuit device. Yuki discloses in figure 3a providing a semiconductor substrate (21). Yuki discloses in figure 3b forming a gate oxide (23) on the semiconductor substrate. Yuki discloses in figure 3b forming a gate (24) on the gate oxide. Yuki discloses in figure 3b implanting a first pocket implant (right side of 21a) and a second pocket implant (left side of 21a) into the semiconductor substrate using the gate as a mask. Yuki discloses in column 5, lines 53 – 60 that the pocket implants are boron implants. Yuki is silent to the first pocket implant and the second pocket implant laterally diffusing in the semiconductor substrate.

Sanchez teaches in column 7, lines 40 – 45 lateral diffusion of boron. It would have been obvious to one of ordinary skill in the art at the time of the present invention for the pocket implants of Yuki to diffuse laterally such as the implants of Sanchez because later process steps

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will facilitate the diffusion as stated by Sanchez in column 7, lines 40 – 45. It is therefore obvious that Yuki has diffusing of the first pocket implant and the second pocket implant laterally as shown in figures 4a and 4b the first pocket implant obviously merges with the second pocket implant due to the implant conditions of the original implants and the later processing. It is obvious in the method of Yuki and Sanchez that the lateral diffusion of the pocket implants would adjust a short channel effect of the transistor. Further, it should be noted that the claim limitation “adjusting a short channel effect of the transistor” is an intended use recitation that is not given patentable weight in a method claim.

With regard to claims 36, it should be noted that “wherein the diffusing increases a threshold voltage of the transistor” is an intended use limitation that does not bear any patentable weight within the method claim. Therefore, Yuki and Sanchez read on the claimed invention.

With regard to claim 38, Yuki discloses in figures 3a – 3d a method of fabricating a transistor in an integrated circuit device. Yuki discloses in figure 3a providing a semiconductor substrate (21) having a surface. Yuki discloses in figure 3b forming a gate oxide (23) on the semiconductor substrate surface. Yuki discloses in figure 3b forming a gate (24) on the gate oxide. Yuki discloses in figure 3b implanting a first pocket implant (right side of 21a) and a second pocket implant (left side of 21a) into the semiconductor substrate from the first side of the gate at an angle. Yuki discloses in column 5, lines 53 – 60 that the pocket implants are boron implants. ~~Yuki is silent to the first pocket implant and the second pocket implant laterally~~ diffusing in the semiconductor substrate. Sanchez teaches in column 7, lines 40 – 45 lateral diffusion of boron. It would have been obvious to one of ordinary skill in the art at the time of the present invention for the pocket implants of Yuki to diffuse laterally such as the implants of

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Sanchez because later process steps will facilitate the diffusion as stated by Sanchez in column 7, lines 40 – 45. It is therefore obvious that Yuki has diffusing of the first pocket implant and the second pocket implant laterally as shown in figures 4a and 4b the first pocket implant obviously merges with the second pocket implant due to the implant conditions of the original implants and the later processing. It should be noted that the claim limitation “adjusting a short channel effect of the transistor” is an intended use limitation which does not bear any patentable weight within the method claim. Therefore, Yuki and Sanchez read on the claimed invention.

With regard to claim 40, Yuki discloses in figure 3b wherein the first pocket implant and the second pocket implant are implanted using the gate as a mask.

With regard to claim 42, Yuki discloses in figures 3a – 3d a method of fabricating a transistor in an integrated circuit device. Yuki discloses in figure 3a providing a semiconductor substrate (21). Yuki discloses in figure 3b forming a gate oxide (23) on the semiconductor substrate. Yuki discloses in figure 3b forming a gate (24) on the gate oxide. Yuki discloses in figure 3b implanting a first pocket implant (right side of 21a) and a second pocket implant (left side of 21a) into the semiconductor substrate from the first side of the gate at an angle. Yuki discloses in column 5, lines 53 – 60 that the pocket implants are boron implants. Yuki is silent to the first pocket implant and the second pocket implant laterally diffusing in the semiconductor substrate. Sanchez teaches in column 7, lines 40 – 45 lateral diffusion of boron. It would have been obvious to one of ordinary skill in the art at the time of the present invention for the pocket implants of Yuki to diffuse laterally such as the implants of Sanchez because later process steps will facilitate the diffusion as stated by Sanchez in column 7, lines 40 – 45. It is therefore obvious that Yuki has diffusing of the first pocket implant and the second pocket implant

laterally as shown in figures 4a and 4b the first pocket implant obviously merges with the second pocket implant due to the implant conditions of the original implants and the later processing. It should be noted that "adjusting a short channel effect of the transistor" is an intended use limitation that does not bear any patentable weight within the method claim. Therefore, Yuki and Sanchez read on the claimed invention.

With regard to claims 43, it should be noted that "wherein the diffusing increases a threshold voltage of the transistor" is an intended use limitation that does not bear any patentable weight within the method claim. Therefore, Yuki and Sanchez read on the claimed invention.

7. Claim 37 and 44 – 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yuki and Sanchez as applied to claims 35, 38, and 42, respectively, above, and further in view of Okumura.

With regard to claims 37 and 44, Yuki and Sanchez teach forming transistors with pocket implants. Yuki and Sanchez do not disclose implanting an enhancement implant. Okumura teaches in figure 6 implanting an enhancement implant (63) in the semiconductor substrate. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the enhancement implant of Okumura in the method of Yuki and Sanchez in order to control the threshold voltage of the device as stated by Okumura in column 6, lines 56 – 62.

With regard to claims 45 – 47, Yuki discloses a well region (21). Yuki and Sanchez do not teach implanting a field implant, a well implant or an enhancement implant. Okumura discloses in figure 6 implanting a field implant (63). Okumura discloses in figure 5 implanting a well implant (62). Okumura discloses in figure 4 implanting an enhancement implant (61).

Okumura discloses in figures 4 – 6 wherein the implanting the field implant, the well implant, and the enhancement implant are done using a single mask (4). It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the single mask method and three implants of Okumura in the method of Yuki and Sanchez in order to suppress substrate bias effects thus improving device performance as stated by Okumura in column 1, lines 12 – 16.

Response to Arguments

8. Applicant's arguments filed February 3, 2004 have been fully considered but they are not persuasive.

9. With regard to applicant's argument that "It is well known in the art that two types of resist may be use when forming layers. One is positive, while the other is negative. With the first, resist is removed where there is an opening in a mask, while with the second, resist remains where there is an opening. Accordingly, one skill in the art will appreciate that region 410 may be an opening, in which case positive resist is appropriate, or mask region 410 may be opaque, in which case negative resist is appropriate. The most important feature is the boundary of mask 410 which is clearly shown in figure 4. The enhancement region is similarly implanted." It is clear that this description used by the applicant defines the use of at least two resist masks, one in the region defined by 410 for implanting the field implants 120, and a second in the region defined outside of 410 for implanting regions 140 and 130. While applicant now defines that one master mask defines two different types of resist in order to define two opposite resist

masks, there is absolutely no disclosure in the originally filed specification that would suggest to one of ordinary skill in the art that the claimed mask is not the actual mask used to block a portion of the substrate during the three implantation steps. In other words, applicant has not disclosed one master mask to define two resist masks. Applicant's argument is clearly an attempt to introduce new matter by way of arguments. Arguments cannot take the place of written description in the originally filed disclosure. Therefore, applicant's arguments are not persuasive, and the rejection is proper.

10. With regard to applicant's argument that Sanchez "teaches away from diffusing the pocket implants laterally. Specifically, Sanchez discusses minimizing lateral diffusion by using lower temperatures and shorter process times. (See Sanchez, column 7, lines 44-46.)" It should be noted that while Sanchez teaches minimizing lateral diffusion, lateral diffusion is still occurring. Further, two references should be used in a "teaching against" argument (i.e. reference A teaches against reference B). Thus, Sanchez cannot teach against itself when it comes to the fact that lateral diffusion does occur. Therefore, applicant's arguments are not persuasive, and the rejection is proper.

11. With regard to applicant's argument that "Here the prior art, specifically Sanchez, teaches how to minimize lateral diffusion. In contrast, the claim recites 'adjusting a short channel effect of the transistor by diffusing the first pocket implant and the second pocket implant laterally in the semiconductor substrate.' Applicants assert that 'minimizing' and 'adjusting' result in a manipulative difference."

12. In response to applicant's argument that "Here the prior art, specifically Sanchez, teaches how to minimize lateral diffusion. In contrast, the claim recites 'adjusting a short channel effect of the transistor by diffusing the first pocket implant and the second pocket implant laterally in the semiconductor substrate.' Applicants assert that 'minimizing' and 'adjusting' result in a manipulative difference", a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963). It further should be noted that the minimized lateral diffusion disclosed by Sanchez would result in adjusting a short channel effect when taken into account in the proposed combination. Thus, there is no manipulative difference between the "adjusting" and "minimizing" because the end result would be the same. Therefore, applicant's arguments are not persuasive, and the rejection is proper.

Conclusion

13. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO**

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MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

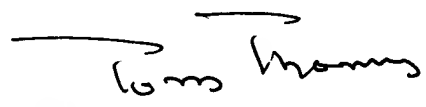
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E Brock II whose telephone number is (571) 272-2723. The examiner can normally be reached on 8:30 AM - 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1164. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Paul E Brock II
March 5, 2004




Tom Thomas
Supervisory Patent Examiner
Technology Center 2800